Claims

1. A circuit, comprising:

a driven half-bridge inverter having an upper transistor, a lower transistor, and a driver circuit for commutating the upper transistor and the lower transistor in a substantially complementary manner;

a resonant output circuit coupled between the inverter and a load;

a control circuit coupled between the resonant output circuit and the driver circuit, wherein the control circuit is operable:

(i) to monitor a signal within the resonant output circuit;

(ii) in response to the signal within the resonant output circuit reaching a predetermined level, to direct the driver circuit to render the upper transistor conductive and the lower transistor non-conductive for a predetermined first period; and

(iii) upon completion of the first period, to direct the driver circuit to render the upper transistor non-conductive and the lower transistor conductive for a second period, wherein the second period ends when the signal within the resonant output circuit again reaches the predetermined level.

2. The circuit of claim 1, wherein the control circuit comprises:

a phase detector circuit having a detector input and a detector output, wherein the detector input is coupled to the resonant output circuit, the phase detector circuit being operable, in response to the monitored signal within the resonant output circuit reaching the predetermined level, to generate a trigger signal at the detector output;

a one-shot circuit coupled between the detector output and the driver circuit, the one-shot circuit being operable, in response to the trigger signal, to direct the driver circuit to render the upper transistor conductive for the first period.

3. The circuit of claim 2, wherein the phase detector circuit is further operable to generate the trigger signal by causing the voltage at the detector output to fall below a predetermined trigger threshold.

4. The circuit of claim 3, wherein the phase detector is further operable such that, after the voltage at the detector output falls below the predetermined trigger threshold, the voltage at the detector output recovers and exceeds the predetermined trigger threshold within a time that is substantially less than the first period.

5. The circuit of claim 2, wherein the one-shot circuit includes a control output that is coupled to the driver circuit, the one-shot circuit being operable, in response to the trigger signal, to generate a control voltage at the control output.

6. The circuit of claim 5, wherein the control voltage has a duration that is approximately equal to the first period.

7. The circuit of claim 2, wherein:

the phase detector circuit generates the trigger signal by causing the voltage at the detector output to fall below a predetermined trigger threshold;

the phase detector is further operable such that, after the voltage at the detector output falls below the predetermined trigger threshold, the voltage at the detector output increases and exceeds the predetermined trigger threshold within a time that is substantially less than the first period;

the one-shot circuit includes a control output that is coupled to the driver circuit, the one-shot circuit being operable, in response to the trigger signal, to generate a control voltage at the control output, the control voltage having a duration that is approximately equal to the first period.

8. The circuit of claim 2, wherein:

the inverter further comprises:

first and second input terminals for receiving a source of substantially direct current (DC) voltage, the second input terminal being coupled to circuit ground;

an inverter output terminal, wherein the upper transistor is coupled between the first input terminal and the inverter output terminal, and the lower transistor is coupled between the inverter output terminal and circuit ground;

the driver circuit includes a control input that is coupled to the one-shot circuit;

the resonant output circuit comprises:

first and second output connections adapted for connection to the load;

a resonant inductor coupled between the inverter output terminal and the first output connection;

a resonant capacitor coupled between the first output connection and circuit ground, the resonant capacitor having a voltage thereacross;

a startup resistor coupled between the first input terminal of the inverter and the first output connection; and

a direct current (DC) blocking capacitor coupled between the second output connection and circuit ground;

the monitored signal within the resonant output circuit is the voltage across the resonant capacitor.

9. The circuit of claim 8, wherein:

the detector input of the phase detector circuit is coupled to the first output connection of the resonant output circuit; and

the phase detector circuit is operable to generate the trigger signal shortly after the voltage across the resonant capacitor reaches its most negative level.

10. The circuit of claim 2, wherein the phase detector circuit further comprises:

a transistor having a base, a collector, and an emitter, the emitter being coupled to circuit ground;

a first capacitor coupled between the detector input and the transistor base;

a diode having a cathode coupled to the transistor base and an anode coupled to circuit ground;

a first resistor coupled between the transistor base and circuit ground;

a second resistor coupled between the detector output and a direct current (DC) supply voltage;

a second capacitor coupled between the detector output and the transistor collector; and

a third resistor coupled in parallel with the second capacitor.

11. The circuit of claim 2, wherein the one-shot circuit comprises a 555 type timer that is operated in a monostable mode.

12. The circuit of claim 2, wherein the one-shot circuit comprises:

a timer integrated circuit that is operated in a monostable mode, the timer integrated circuit including: (i) a trigger input that is coupled to the detector output of the phase detector circuit; (ii) an output that is coupled to the driver circuit of the inverter; and (iii) a timing input; and

a timing network that determines the first period, comprising:

a timing resistance coupled between the DC supply voltage and the timing input of the timer integrated circuit; and

a timing capacitance coupled between the timing input and circuit ground.

13. The circuit of claim 12, wherein:

the timing resistance is adjustable;

an increase in the timing resistance increases the first period; and

a decrease in the timing resistance decreases the first period.

14. The circuit of claim 1, wherein the load comprises at least one discharge lamp.

15. A circuit comprising:

an inverter, comprising:

first and second input terminals for receiving a source of substantially direct current (DC) voltage, the second input terminal being coupled to circuit ground;

an inverter output terminal;

a first inverter transistor coupled between the first input terminal and the output terminal;

a second inverter transistor coupled between the inverter output terminal and circuit ground; and

a driver circuit coupled to the first and second inverter transistors, the driver circuit having a control input for receiving a control voltage that varies between a low level and a high level, wherein the driver circuit is operable: (i) in response to the control voltage being at the high level, to cause the first inverter transistor to be on and the second inverter transistor to be off; and (iii) in response to the control voltage being at the low level, to cause the first inverter transistor to be off and the second inverter transistor to be on;

an output circuit, comprising:

first and second output connections adapted for connection to a load;

a resonant inductor coupled between the inverter output terminal and the first output connection;

a resonant capacitor coupled between the first output connection and circuit ground;

a startup resistor coupled between the first input terminal of the inverter and the first output connection; and

a direct current (DC) blocking capacitor coupled between the second output connection and circuit ground;

a control circuit coupled between the first output connection of the output circuit and the control input of the driver circuit, the control circuit being operable:

(a) to monitor the voltage across the resonant capacitor;

(b) in response to the voltage across the resonant capacitor reaching a predetermined level, to set the control voltage at the high level for a predetermined first period; and

(c) upon completion of the predetermined period, to set the control voltage at the low level and maintain the control voltage at the low level for a second period, wherein the second period ends when the voltage across the resonant capacitor again reaches the predetermined level.

16. The circuit of claim 15, wherein the control circuit comprises:

a phase detector circuit having a detector input and a detector output, wherein the detector input is coupled to the first output connection of the output circuit, the phase detector circuit being operable, in response to the voltage across the resonant capacitor reaching the predetermined level, to generate a trigger signal at the detector output, the trigger signal having a duration that is substantially less than the first period; and

a one-shot circuit coupled between the detector output and the driver circuit, the one-shot circuit having a control output coupled to the control input of the driver circuit, the one-shot circuit being operable: (i) in response to the trigger signal, to cause the control voltage to go to the high level for the first period; and (ii) upon completion of the predetermined period, to cause the control voltage to go to the low level and to maintain the control voltage at the low level until such time as another trigger signal is provided by the phase detector at the detector output.

17. The circuit of claim 16, wherein the phase detector circuit further comprises:

a transistor having a base, a collector, and an emitter, the emitter being coupled to circuit ground;

a first capacitor coupled between the detector input and the transistor base;

a diode having a cathode coupled to the transistor base and an anode coupled to circuit ground;

a first resistor coupled between the transistor base and circuit ground;

a second resistor coupled between the detector output and a direct current (DC) supply voltage;

a second capacitor coupled between the detector output and the transistor collector; and

a third resistor coupled in parallel with the second capacitor.

18. The circuit of claim 16, wherein the one-shot circuit further comprises:

a timer integrated circuit that is operated in a monostable mode, the timer integrated circuit including: (i) a trigger input that is coupled to the detector output of the phase detector circuit; (ii) an output that is coupled to the control output; and (iii) a timing input; and

a timing network that determines the first period, comprising:

a timing resistance coupled between the DC supply voltage and the timing input of the timer integrated circuit; and

a timing capacitance coupled between the timing input and circuit ground.

19. The circuit of claim 15, wherein the load comprises at least one discharge lamp.

20. A circuit, comprising:

an inverter, comprising:

first and second input terminals for receiving a source of substantially direct current (DC) voltage, the second input terminal being coupled to circuit ground;

an inverter output terminal;

a first inverter transistor coupled between the first input terminal and the output terminal;

a second inverter transistor coupled between the inverter output terminal and circuit ground; and

a high-side driver circuit coupled to the first and second inverter transistors, the high-side driver circuit having a control input (202) for receiving a control voltage that varies between a low level and a high level, wherein the high-side driver circuit is operable: (i) in response to the control voltage being at the high level, to cause the first inverter transistor to be on and the second inverter transistor to be off; and (iii) in response to the control voltage being at the low level, to cause the first inverter transistor to be off and the second inverter transistor to be on;

an output circuit, comprising:

first and second output connections adapted for connection to a load;

a resonant inductor coupled between the inverter output terminal and the first output connection;

a resonant capacitor coupled between the first output connection and circuit ground;

a startup resistor coupled between the first input terminal of the inverter and the first output connection; and

a direct current (DC) blocking capacitor coupled between the second output connection and circuit ground;

a phase detector circuit, comprising:

a detector input coupled to the first output connection of the output circuit;

a detector output;

a transistor having a base, a collector, and an emitter, the emitter being coupled to circuit ground;

a first capacitor coupled between the detector input and the transistor base;

a diode having a cathode coupled to the transistor base and an anode coupled to circuit ground;

a first resistor coupled between the transistor base and circuit ground;

a second resistor coupled between the detector output and a direct current (DC) supply voltage;

a second capacitor coupled between the detector output and the transistor collector; and

a third resistor coupled in parallel with the second capacitor.

a one-shot circuit, comprising:

a control output coupled to the control input of the high-side driver circuit;

a timer integrated circuit that is operated in a monostable mode, the timer integrated circuit including: (i) a trigger input that is coupled to the detector output of the phase detector circuit; (ii) an output that is coupled to the control output; and (iii) a timing input; and

a timing network, comprising:

a timing resistance coupled between the DC supply voltage and the timing input of the timer integrated circuit; and

a timing capacitance coupled between the timing input and circuit ground.